

REMARKS

The November 13, 2008 Advisory Action was based on pending Claims 1–11, with Claim 1 being the only independent claim.

Applicant thanks the Examiner for the careful and thoughtful consideration of Applicant's previous arguments and amendments submitted in Applicant's Amendment filed October 21, 2008.

By way of this Response, no claim amendments are being presented, and Applicant respectfully requests reconsideration of the pending claims in view of the remarks set forth below.

SUMMARY OF NOVEMBER 13, 2008 ADVISORY ACTION

The Advisory Action indicates that Applicant's Amendment filed October 21, 2008, does not place the application in condition for allowance, and the claims continue to be rejected as being obvious over U.S. Patent No. 6,069,386 to Jos ("Jos") in view of U.S. Patent No. 6,294,798 to Zambrano ("Zambrano"). In particular, the Advisory Action states that Applicant's previous arguments are not persuasive because "Zambrano teaches a capacitor (5) between a metal source contact (16) and a further metal strip (28)" based on Figure 1 and column 3, lines 38–41 of Zambrano.

RESPONSE TO ADVISORY ACTION

The August 21, 2008 Final Office Action and the Advisory Action acknowledge that Jos does not teach or suggest attaching a capacitor between a further metal strip and a source contact. Rather, a combination of Jos and Zambrano is cited for teaching this claim element.

Zambrano teaches forming a circuit structure on a semiconductor substrate, which comprises electronic devices formed with both CMOS technology elements and capacitor elements (see, e.g., col. 1, line 58 through col. 2, line 12). Zambrano thereby aspires to form an integrated circuit with contact areas with a low aspect ratio and better integrated so that the overall circuit structure is more compact relative to prior art (see, e.g., col. 1, lines 58–65).

The Advisory Action further cites the following text of Zambrano (i.e., col. 3, lines 38–41) and Figure 1 (reproduced below)) for teaching placing a capacitor (5) between a metal source contact (16) and a further metal strip (28):

Openings 27 and 25 are defined in this oxide layer 19, respectively above and adjacent to the contact 17 of the drain region 7 and the top electrode 10 of the capacitor element 5.

Finally, a metallization layer 28 functions to connect these regions electrically.

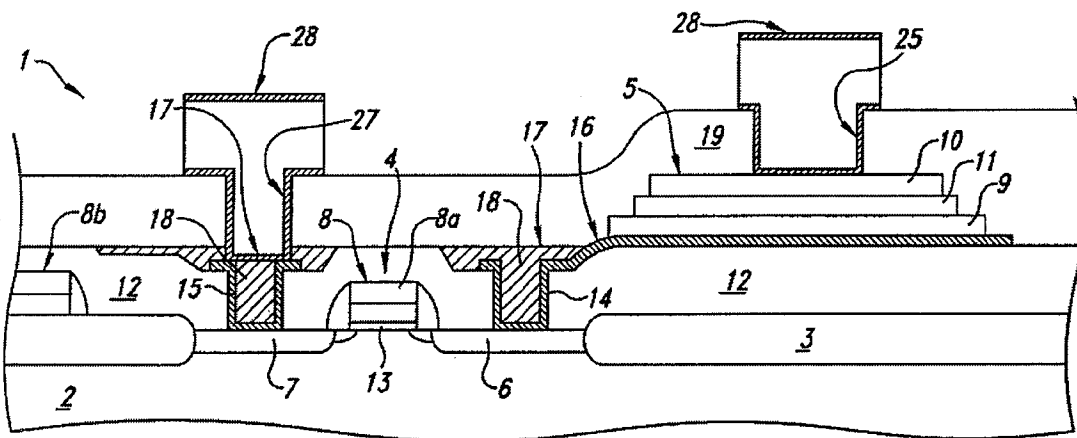


Fig. 1

In view of the foregoing, Applicant respectfully submits that Claims 1–11 are patentably distinguished over the art of record because: (1) there is no reasonable expectation of success in the proposed combination of Jos and Zambrano to teach the claimed invention; and (2) there is no further suggestion or motivation to combine Jos and Zambrano.

There is No Reasonable Expectation of Success in the Proposed Combination of Jos and Zambrano

A *prima facie* case of obviousness requires that there be a reasonable expectation of success in combining the teachings of the prior art (see, e.g., M.P.E.P. § 2143.02(I) stating that “[t]he prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success”).

Independent Claim 1 requires “wherein a further metal strip is positioned between the gate electrode contact and the drain contact.”

Zambrano, on the other hand, teaches positioning a metallization layer (28) above a capacitor element (5) on the top of a semiconductor (see, e.g., Fig. 1) for connecting the region electrically (see, e.g., col. 3, lines 41–42). Zambrano does not teach or suggest positioning a further metal strip between a gate electrode contact (8) and a drain contact (7), as required by independent Claim 1.

Jos appears to teach placing a further metal strip between a gate electrode contact and a drain contact but does not teach the addition of a capacitor.

It is not clear how it would be possible to place the Zambrano's metallization layer (28), which is connected by a capacitor element (5) to the source (6), between the gate electrode contact (8) and the drain contact (7) according to the teachings of Jos. None of the figures or disclosures of Zambrano or Jos, nor the knowledge of a skilled artisan, provides a solution to this problem. Only from Applicant's disclosure is such a solution provided (see, e.g., Figures 3 and 5).

There is No Further Suggestion or Motivation to Combine Jos and Zambrano

Jos does not suggest that its teachings are unsatisfactory and does not provide any motivation to search for an improvement to its teachings. Applicant further submits that it would not have been obvious to one skilled in the art to add a capacitor to achieve better results, or to determine that a capacitor would provide such an improvement, such as the results presented in Applicant's specification (see, e.g., Figures 6–8; and page 8, line 9, through page 9, line 34).

Zambrano does not suggest adding capacitors to circuits but rather creating circuits containing a capacitor in semiconductor form. Jos does not teach a capacitor between the source and the further metal strip, so Zambrano would have no reason to add one.

Summary

Because the cited references cannot be properly combined to teach the claimed invention, Applicant asserts that Claim 1 is not obvious in view of Jos and Zambrano, and Applicant respectfully requests allowance of Claim 1.

Moreover, Claims 2–11 depend from independent Claim 1 and are believed to be further patentably distinguished over the cited references for the additional features recited therein.

NO DISCLAIMERS OR DISAVOWALS

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain, the Examiner is cordially invited to contact the undersigned such that the issues may be promptly resolved.

Moreover, by the foregoing remarks no admission is made that any of the above-cited references are properly combinable. Rather, Applicant submits that even if the references are combined, the references still do not teach or suggest the claimed invention.

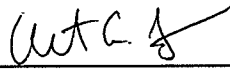
Application No.: 10/551,324
Filing Date: October 18, 2005

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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